28. An error correction device which performs error correction for data in ECC blocks each having a structure where error correcting code words each comprising a data unit and a parity unit are arranged in vertical and

5   horizontal directions so as to realize repeated error correction, and predetermined data composed of a predetermined number of code words in the vertical or horizontal direction (data in the horizontal direction are referred to as sector) are as one unit subjected to error correction, and which also perform syndrome calculation and error detection in parallel

10   with a storage of demodulated codes in a buffer memory, said error correction device comprising:

a first syndrome calculating means for performing syndrome calculation with said buffer memory;

a first error detecting means which pairs up with the first syndrome

15   calculating means;

a second syndrome calculating means for performing syndrome calculation of demodulated codes without said buffer memory;

a second error detecting means which pairs up with the second syndrome calculating means;

20   a storing means for storing mid-term results of calculations of the first error detecting means and the second error detecting means;

a buffer memory parallel transfer means for transferring data transmitted from upstream to the second syndrome calculating means and to the second error detecting means in parallel with storage of the data in

25   said buffer memory until the second syndrome calculating means detects

an error-containing code;

an error-detecting-means switch means for switching between the first error detection means and the second error detection means in a manner that after the second syndrome calculating means detects an error-containing code, said storing means is provided with the mid-term results of the calculation by the second error detecting means of code words until said error-containing code is detected, and on and after the second-time error correction in a same direction, after the second syndrome calculating means detects an error-containing code, said storing means is provided with the mid-term results of the calculation by the second error detecting means of code words until said error-containing code is detected;

an error correcting means for performing error correction after one of the first error detecting means and the second error detecting means detects an error-containing code word;

a parallel transfer means for, on and after the second-time error correction in the same direction, before the first syndrome calculating means detects an error-containing code, transferring data stored in said buffer memory, starting at a code word which is not stored in said storing means to the first syndrome calculating means and to the first error detecting means; and

a second-time onward detecting-processed data use means for, on and after the second-time error detection in the same direction done by the second error detecting means, performing error detection of the subsequent code words by using the mid-term results stored in said storing means.

29. An error correction device which performs error correction for data in ECC blocks each having a structure where error correcting code words each comprising a data unit and a parity unit are arranged in vertical and horizontal directions so as to realize repeated error correction,

5   and predetermined data composed of a predetermined number of strings in the vertical or horizontal direction (data in the horizontal direction are referred to as sector) are as one unit subjected to error correction, and which also perform syndrome calculation and error detection in parallel with a storage of demodulated codes in a buffer memory, said error

10   correction device comprising:

a first syndrome calculating means for performing syndrome calculation with said buffer memory;

a first error detecting means which pairs up with the first syndrome calculating means;

15   a second syndrome calculating means for performing syndrome calculation of demodulated codes without said buffer memory;

a second error detecting means which pairs up with the second syndrome calculating means;

a storing means for storing mid-term results of calculations of the

20   first error detecting means and the second error detecting means in predetermined data units such as ECC block units, sector units, and sector group units;

a buffer memory parallel transfer means for transferring data transmitted from upstream to the second syndrome calculating means and

25   to the second error detecting means in said data units in parallel with